

Name: \_\_\_\_\_ Date: \_\_\_\_\_

**Objectives:**

- To construct and evaluate a MOD 16 counter built from a 74LS293 IC – Decade and 4-Bit Binary Counters
- To develop a block diagram for a 24-hour digital clock.
- To design, construct, and evaluate a 24-hour clock.

**Suggested Reading**

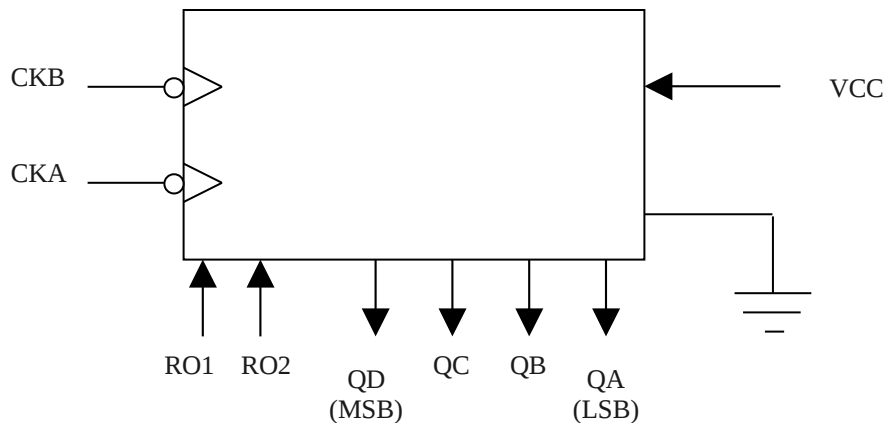
Chapter 7, Digital Systems, Principals and Applications; Tocci

**Equipment:**

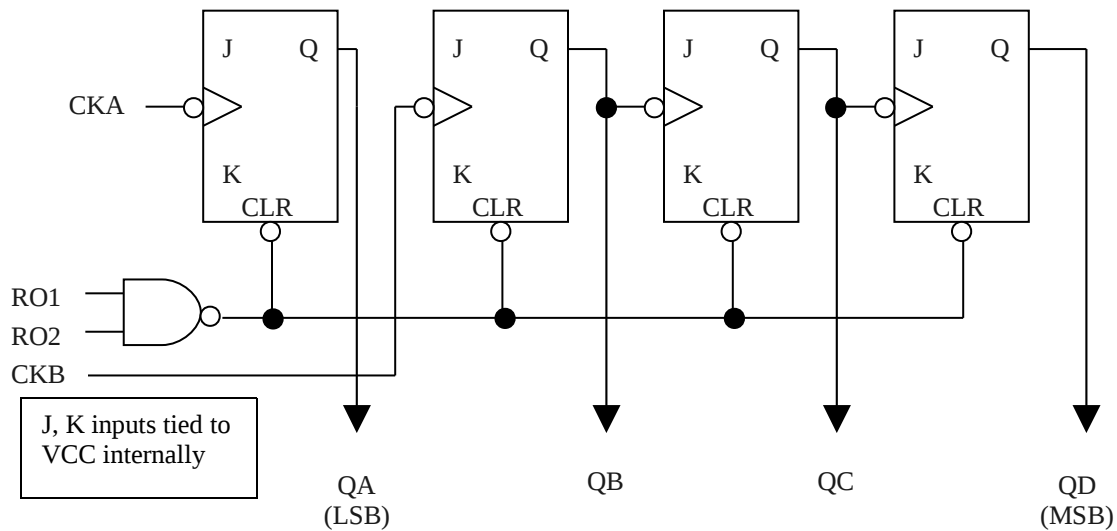
Circuit simulator (MultiSIM or an equivalent)

**Introduction:**

74LS293 is an asynchronous ripple counter. Each device provides circuitry for a 3-bit counter, 4-bit counter, or divide by 2 circuit. The block and logic diagrams are shown in the following figures.



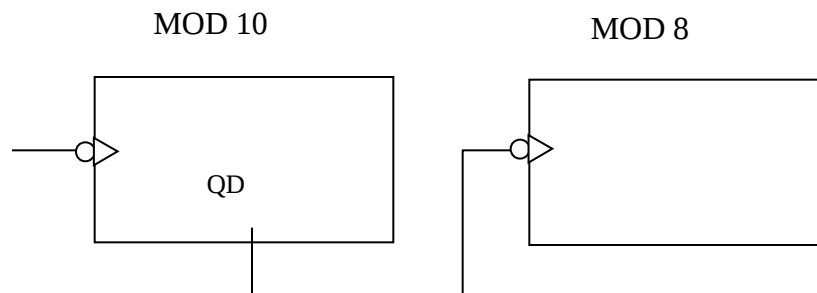
**74LS293 Block Diagram**



**Logic Diagram for 74LS293**

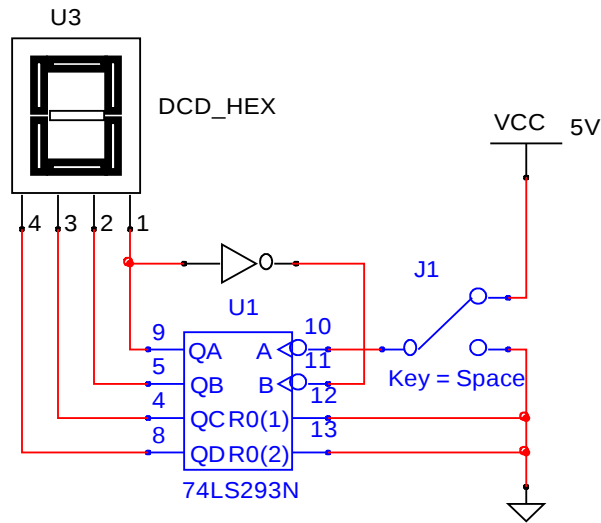
The 74LS293 has four J-K flip-flops with outputs QA, QB, QC, and QD, where QA is the LSB and QD is the MSB. Each flip-flop has an asynchronous active-low CLEAR line that is connected to the output of a 2-input NAND gate. The NAND gate is used to create counters with a MOD number less than the maximum MOD ( $2^N$ ). Flip-flops QB, QC, and QD are connected as a 3-bit ripple counter. Flip-flop QA is not connected to the other flip-flops and can be used as a single divide-by-two circuit. There are clock inputs for both QA and the 3-bit counter circuit. If a counter with a MOD number greater than 8 is required, the output QA can be connected externally to CKB input to create a 4-bit ripple counter circuit. In this case, only the CKA input is the clock for the circuit. If a counter requires more than 2 of the outputs to be connected to the NAND gate, an external AND gate must be added to one of the NAND gate inputs.

Counters with a MOD number larger than 16 can be created by cascading 74LS293 counters. The MOD number is equal to the product of the individual MOD numbers. For example, a MOD 80 counter can be implemented as shown in the following figure (general block diagram, all of the wiring is not shown).



**Procedure:**

- Construct the following MOD 16 counter in MultiSIM. Note that the output QA is tied to the CKB clock input through an inverter to implement a 4-bit ripple counter. [The inverter is required due to a model error in the Multisim simulation. The CKB model input is not NGT as the schematic symbol implies. The inverter must be used in your subsequent counter designs.]



- Record the display value for each clock (falling edge) in the following table.

Clock	Display Value
0	0
1	
2	
3	
4	
5	
6	
7	
8	
9	
10	
11	
12	
13	
14	
15	



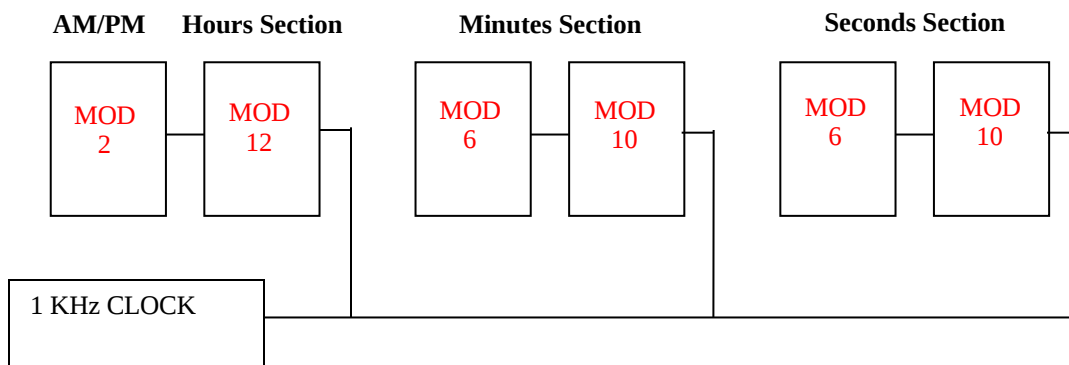
counter 11 (1011) corresponds to the display 12 due to the adder, use an AND gate to decode the 11 to provide the rising edge to trigger the AM/PM flip-flop.

10. It is quicker to run two identical MOD 60 counters from the same clock instead of waiting for the seconds to trigger the minutes. Also run the MOD 12 + AM/PM directly from the clock to save time.

**Label the schematic so that each section (seconds, minutes, hours, etc.) and MOD number of each counter can be clearly identified.**

**Demonstrate the operation of the circuit to your instructor, when approved print a copy of the schematic.**

**ATTACH A COPY OF THE MULTISIM SCHEMATIC TO THE LAB.**



**Review Questions:** Answer the following questions after the lab is completed.

1. What is the advantage of using a 74LS293 component versus constructing a MOD 16 counter out of discrete J-K flip-flops?
2. What is the largest MOD counter that can be implemented by cascading two 74LS293 components together?
3. What is the MOD number of the 74LS293 circuit shown below?

